**DDCO LAB WEEK2 SUBMISSION FORMAT**

**Read the below instructions before submission of WEEK2 DDCO Lab Programs. All 4 programs to be submitted in a single pdf file and name the file as DDCOLAB2\_PES2UG19CSxxx\_STUDENTNAME\_SECTION.pdf**

**PROGRAM 1**

**AIM: DESIGN A FULL ADDER USING BASIC GATES AND VERIFY THE FULL ADDER TRUTH TABLE**

1. Complete the code provided in the fulladd.v (source File) and execute it using the iverilog command along with the related testbench.

2. Your Submission should include the screenshot

1. the source code file
2. the output of the VVP command
3. GTKWAVE waveform

**PROGRAM 2**

**AIM: DESIGN A FOUR BIT RIPPLE CARRY ADDER USING FULL ADDER CODE**

1. Complete the code provided in the rca.v (source File) and execute it using the iverilog command along with the related testbench.

2. Your Submission should include the screenshot

1. the source code file
2. GTKWAVE waveform
3. The truth table in the adders PPT has to be completed after verifying the values in the GTK wave waveform.

**PROGRAM 3**

**AIM: DESIGN A 2 TO 1 MULTIPLEXER AND VERIFY ITS TRUTH TABLE**

1. Complete the code provided in the mux2to1.v (source File) and execute it using the iverilog command along with the related testbench.

2. Your Submission should include the screenshot

1. the source code file
2. GTKWAVE waveform
3. The truth table of 2 to 1 multiplexers has to be completed after verifying the values in the GTK wave waveform.

**PROGRAM 4**

**AIM: DESIGN A 4 TO 1 MULTIPLEXER AND VERIFY ITS TRUTH TABLE**

1. Complete the code provided in the mux4to1.v (source File) and execute it using the iverilog command along with the related testbench.

2. Your Submission should include the screenshot

1. the source code file
2. GTKWAVE waveform
3. The truth table of 4 to 1 multiplexers has to be completed after verifying the values in the GTK wave waveform